Serial Nr.: 09/627,979
Art Unit: 2814

UPA-00156

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	**09/627,979**	Examiner:	**DiLinh Nguyen**
Inventor:	**Randy H. Y. Lo, Chi-Chuan Wu and Ssu-Cheng Lai**		
Filed:	**July 28, 2000**	Art Unit:	**2814**
Title:	**Method Of Packaging Multi Chip Module**		

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REMARKS

This is a response to the Office Action mailed on 07/01/2003. In the Office Action, the examiner stands on the rejection based on the same ground stated in the office mailed on 3/14/2003. **It is clear that the examiner might not have considered the arguments presented on 6/8/2003 by the applicants**.

Claims 41-45 and 47-48 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lin and Akram et al. in view of Rostoker et al. Claims 49-54 and 56-57 are rejected under 35 U.S.C. §103(a) as being unpatentable over Tanioka in view of Rostoker et al. Applicants respectfully contend that the instant invention is patentable over the cited prior arts and petition that the examiner considers Applicants' arguments made in the Amendment D and the remarks in this response.

In the following discussion, the teaching of the prior arts cited by the examiner will be more specifically excerpted and compared with the examiner's comments to elucidate the difference between the prior arts and the instant invention.

Rejection of claims 41-45 and 47-48 under 35 U.S.C. §103(a)

On page 2 of the office action, the examiner states that "Lin discloses a multi-chip module package structure (fig. 1A, col. 1, lines 33), ..., wherein the multi-chip module package structure is a ball grid array package (fig. 2A, col. 4, line 29)".

Referring to the specification of Lin, "In Fig. 1A, three of these packaged CSP of Figs. 1A-a are mounted on a **multiple-chip-module (MCM) board.**" (col. 1, lines 40-42). "The MCM module 100 includes multiple flip chips, e.g. chips 120-1 to 120-3 mounted on a **printed circuit board** 110." (col. 4, lines 21-23). It can be seen that the examiner statement is unwarranted because Lin only discloses **multiple-chip-module board** and **printed circuit board**. Neither multi-chip module **package** nor ball grid **package** has been disclosed.

It should be noted that Lin's invention is aimed at dual in-line memory module (DIMM) or single-in-line-memory module (SIMM) (col. 1, lines 29-31). These types of multiple-chip-modules are totally different from the "**multi-chip module package**" which is in the form of an integrated circuit package as shown in FIGs. 1-3 of the instant invention. The fact that DIMM and SIMM are mounted on a printed circuit board makes it impractical to further package the multiple-chip-module board of this type. Therefore,

nowhere has Lin's disclosure motivated a person skilled in the art to further enclose or package a **multiple-chip-module (MCM) board** or a **printed circuit board** 110.

On pages 2-3 of the office action, the examiner states that "Akram et al. disclose a semiconductor device (cover fig.) comprising a plurality of electrical connect pins 114 (col. 5, line 64), a package material 172 (col. 6, line 26) enclosing a multi-chip module substrate 102, a connect point 126 and a chip package to achieve densely packaged semiconductor device (abstract)".

Referring to col. 6, line 26 and lines 61-62 of Akram et al., what is really disclosed is "Furthermore, an encapsulation material 172 may cover the **stack dice portion** of the stacked assembly 100". Referring further to the abstract of Akram et al., it reads "A semiconductor package comprising multiple stacked substrate having **flip chips** attached to the substrate with **chip on board** assembly techniques to achieve dense package". It is common knowledge for a person with ordinary skill in the art of semiconductor to realize the difference between a chip (bare die) and a chip package. Applicants respectfully contend that the examiner's statement is unwarranted because all the disclosure of Akram et al. only refers to **chip or chip on board** which is certainly different from a **chip package**.

In short, the key subject matter in the art of Akram et al. is to stack multiple substrates of bare chips in the vertical direction to achieve high density. It is clear that the teaching is to cover the "dice portion". There is absolutely no teaching or suggestion to enclose or package **a multi-chip substrate and individually packaged chip packages** as claimed in claim 41.

Rostoker et al. disclose a technique for individually electronically selecting unsingulated dies on a wafer for testing. The disclosed art does not teach or suggest any multi-chip module packaging. Applicants also like to point out that the art of Rostoker et al. is for **testing unsingulated dies** on a wafer that is completely different from the art of **testing a chip scale package** in the semiconductor industry. As recited in claim 41, "**said at least two chip packages having been burn-in tested and function tested**" is the subject matter of this invention that is very different from the teaching of Rostoker et al.

As pointed out in the specification of the instant invention and previous amendments, the gist of this invention is to **package a multi-chip module that encloses individually packaged chips into a ball grid array package**, and hence the package structure of the invention as recited in claim 41 is invented.

From the above discussion, it is evident that none of the cited prior arts disclose or suggest **packaging a multi-chip substrate and individually packaged chip packages that are burn-in tested and function tested** of claim 41. Applicants respectfully submit that claim 41 has overcome the rejection under U.S.C. §103(a) over Lin and Akram et al. in view of Rostoker et al. Claims 41-45 and 47-48 should be allowable.

Rejection of claims 49-54 and 56-57 under 35 U.S.C. §103(a)

On page 4 of the office action, the examiner states that "Tanioka discloses a multi-chip module package structure (fig. 1, col. 1, lines 39 et seq.) comprising a multichip module substrate 10 (col. 1, line 41), at least a bare chip 7, at least one chip package being **a packaged chip module** having a bare chip 2 and a chip substrate

packaged 11 and enclosed therein, ...".

Referring to the true disclosure of Tanioka, "In the first prior art example shown in FIG. 1, a thin multi-layer board 11 is formed on a thick multi-layer board 10, and a multi-layer hybrid circuit is formed by the wire-bonding 15 of **bare chips** 2 and the **mounting of chip parts** 7." (col. 1, lines 39-47). As pointer out before, any person with ordinary skill in the art of semiconductor realizes the difference between a chip (bare die) and a chip package. Throughout the disclosure of Tanioka, there is no mentioning of any chip package disposed on a multi-layer board. Applicants respectfully contend that the examiner's statement is unwarranted because Tanioka only discloses **bare chip** and **the mounting of chip parts** rather than **a packaged chip module.**

In short, Tanioka **does not teach any chip package being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, said at least one chip package having been burn-in tested and function tested**. The bare chip 2 and the multi-layer board 11 **are encapsulated while they are mounted on the multi-layer board 10**. It is not **a chip package having been pre-packaged** and burn-in tested in the package.

As discussed earlier, Rostoker et al. does not teach or suggest any multi-chip module packaging. The art of Rostoker et al. is for **testing unsingulated dies** on a wafer that is completely different from the art of **testing a chip scale package** which is done after the dies have been cut, separated and packaged in the semiconductor industry. As recited in claim 49, "**said at least one chip package having been burn-in tested and function tested"** is the subject matter of this invention that is very different from the

teaching of Rostoker et al.

From FIG. 1 of Tanioka's art, it can be seen that the bare chip 2 and thin multi-layer board 11 are **encapsulated directly above the multi-layer board 10 and the encapsulation material also covers the multi-layer board 10. There does not exist any chip package being a packaged chip module which has been burn-in tested and function tested.** Consequently, the combination of Rostoker et al. and Tanioka can not reach the subject matter of claim 49 that recites "**at least one chip packaging having been burn-in tested and function tested**".

From the above discussion, it is evident that none of the cited prior arts discloses or suggests **packaging a multi-chip substrate and individually packaged chip packages that are burn-in tested and function tested** of claim 49. Applicants respectfully submit that claim 49 has overcome the rejection under U.S.C. §103(a) over Tanioka in view of Rostoker et al. Claims 49-54 and 56-57 should be allowable.

In summary, from the foregoing discussion it is clear that the instant invention differs from the cited prior arts. The physical difference results in different effects and is not obvious. The base claims 41 and 49 have clearly defined the unique feature of this invention and overcome all the rejections under 35 U.S.C. §103(a) and should be patentable. By virtue of dependency, claims 42-45, 47-48 and 50-54, 56-57 should also be patentable. Applicants respectfully request that the examiner consider the above remarks. Prompt and favorable reconsideration of the application is respectfully solicited.

Respectfully submitted,

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